EXHIBIT 1

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND/ODESSA DIVISION

REDSTONE LOGICS LLC, **Plaintiff,** **v.** **NXP USA, Inc.,** **Defendant.**	**Civil Action No. 7:24-cv-00028-DC-DTG** **JURY TRIAL DEMANDED**

DECLARATION OF JOHN VILLASENOR, PH.D.
IN SUPPORT OF
<u>NXP'S OPENING CLAIM CONSTRUCTION BRIEF</u>

Table of Exhibits

Exhibit A	U.S. Patent No. 8,549,339 ('339 Patent)
Exhibit B	ON Semiconductor's application note AND8248/D (*Stys*)
Exhibit C	U.S. Patent No. 7,538,625 (*Cesky*)
Exhibit D	U.S. Pat. App. Pub. No. 2009/0106576 (*Jacobowitz*)
Exhibit E	U.S. Pat. App. Pub. No. 2009/0138737 (*Kim*)
Exhibit F	'339 Patent file history excerpt: Office Action (Aug. 29, 2012)
Exhibit G	'339 Patent file history excerpt: Examiner Interview (Nov. 27, 2012)
Exhibit H	'339 Patent file history excerpt: Applicant's Response to Office Action (Nov. 29, 2012)

I, Dr. John Villasenor, declare that I have personal knowledge of the facts set forth in this declaration and, if called to testify as a witness, could and would do so competently.

I. INTRODUCTION

1. My name is John Villasenor. I have been retained on behalf of NXP USA, Inc. ("Defendant" or "NXP") as an independent expert in the relevant art in connection with the above-captioned case.

2. I have been asked to render opinions regarding technical aspects of the multi-core processors disclosed in U.S. Patent No. 8,549,339 ("the '339 Patent").

3. My work on this matter is being billed at my customary rate of $1000 per hour. Also, I am being reimbursed for reasonable expenses I incur in relation to my services. My compensation does not depend upon the results of my analysis or the substance of my testimony. Nor does my compensation depend on the outcome of any proceeding that my work is used in.

II. QUALIFICATIONS

4. I have either trained or worked in algorithms and architectures for computer processing of data, as well as the design of hardware for complex processing tasks, for approximately three decades. Appendix 1 to this Declaration is a true and correct copy of my Curriculum Vitae, which provides further details about my background and experience, including details regarding my publications, professional awards, and prior testifying experience.

5. My work focuses on innovative, high-performance communications, networking, media processing, and computing technologies and their broader implications. Well before the priority date of the patent in suit, I performed research on the design of processors and the systems in which they are used, including work involving computational logic, memory, and interconnect.

6. I have performed work on mapping complex computational processes into hardware implementations, subject to constraints on factors including speed, area, power consumption, memory access, and the precision of the computations.

7. I received my B.S. in Electrical Engineering from the University of Virginia in 1985, and M.S. and Ph.D. in Electrical Engineering from Stanford University in 1986 and 1989, respectively.

8. While at Stanford, I concentrated my research on digital signal processing and communications.

9. Between 1990 and 1992, I worked for the Jet Propulsion Laboratory in Pasadena, CA, where I helped to develop techniques for imaging and mapping the earth from space. Since 1992, I have been on the faculty of the Electrical Engineering Department of the University of California, Los Angeles (UCLA). Between 1992 and 1996, I was an Assistant Professor; between 1996 and 1998, an Associate Professor; and since 1998, I have been a full Professor.

10. For several years starting in the late 1990s, I served as the Vice Chair of the Electrical Engineering Department at UCLA. In addition to my faculty appointment in the UCLA Samueli School of Engineering, I hold faculty appointments (and have taught classes in) the UCLA School of Law, the Department of Public Policy within the UCLA Luskin School of Public Affairs, and in the UCLA Anderson School of Management. I am also the founder and faculty co-director of the UCLA Institute for Technology, Law, and Policy.

11. In the UCLA Samueli School of Engineering, I have taught courses addressing digital signal processing, communications, computing, and networking, including consideration of the associated systems, algorithms, devices, and networks. In addition to my teaching, I have performed extensive research at UCLA over the past several decades on multiple aspects of digital

devices and systems, including device (including chip) design, integration and use of devices within the context of larger networks; acquisition, processing, and communications of data (including image and video data); communications and protocols used to convey information among devices; optimization to achieve goals including low power consumption and high speed; and mapping of algorithms onto hardware. My work has considered both hardware and software, and has included consideration of factors such as configuration and control of devices, protocols, the interaction among devices, allocation of processing tasks within devices, communication of data to, from, and within devices, and artificial intelligence.

12. My academic publications have appeared in peer-reviewed journals including IEEE Transactions on VLSI Systems, IEEE Transactions on Computers, IEEE Transactions on Reliability, IEEE Transactions on Signal Processing, ACM Computing Surveys, Journal of Statistical Software, IEEE Transactions on Communications, IEEE Transactions on Circuits and Systems for Video Technology, IEEE Transactions on Information Theory, IEEE Transactions on Image Processing, and in numerous peer-reviewed conference proceedings.

13. I am an inventor on approximately 20 issued U.S. patents in areas including information processing, data compression, communications, and cybersecurity. I have published over 175 articles in peer-reviewed journals and academic conference proceedings. I have also been asked on multiple occasions to provide congressional testimony on technology topics.

14. In addition to my work at UCLA, I am a nonresident senior fellow at the Brookings Institution in Washington, D.C. Through Brookings I have examined a wide range of topics at the technology/policy intersection including cybersecurity, wireless mobile devices and systems, and artificial intelligence. In addition to publishing in traditional academic venues such as engineering journals, engineering conference proceedings, and law reviews, I have published papers through

the Brookings Institution and articles and commentary in broader-interest venues including *Billboard*, the *Chronicle of Higher Education*, *Fast Company*, *Forbes*, the *Los Angeles Times*, the *New York Times*, *Scientific American*, *Slate*, and the *Washington Post*.

15. I also have several decades of experience working in early-stage technology ventures. In that capacity, I have met with many companies and evaluated their existing and proposed technology. In multiple instances, I performed work over a multi-year period as a technical consultant to early-stage technology companies, contributing to their efforts to grow their product lines. In multiple cases, this involved work on advanced processing technologies. To take one example, I was a consultant to Broadcom for an extended period of years starting in the early 1990s. In that capacity, I worked on the design of groundbreaking chips for processing communications and multimedia (including video) information, including doing work relating to task allocation, power management, and communication of data to, from, and within such chips. My technology consulting experience has also involved work with other companies developing chips to meet stringent performance and power constraints.

III. MATERIALS CONSIDERED AND RELIED ON

16. In forming my opinions, I have reviewed or relied on:

- The specification, claims, and file history of the ’339 Patent;
- The materials cited in this Declaration; and
- My background and experience in the field of computer processing.

IV. APPLICABLE LEGAL STANDARDS

17. I am not a legal expert and offer no opinions on the law. However, I have been informed by counsel of certain legal standards that apply to claim construction, which I have used in arriving at my conclusions.

A. Claim Construction

18. I understand that claim terms are generally given their ordinary and customary meaning, which is the meaning the terms would have had to a person of ordinary skill in the art ("POSITA") on the effective filing date of the patent. A POSITA is deemed to read the claim term not only in the context of the particular claim in which it appears, but in the context of the intrinsic record, including the specification and prosecution history.

19. I understand that the specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In other cases, the specification may reveal an intentional disclaimer, or disavowal, of claim scope by the inventor.

20. I understand that the prosecution history of a patent can often inform the meaning of the claim language by demonstrating how the applicant understood the invention and whether the applicant limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be. I understand that when the patentee unequivocally and unambiguously disavows a certain meaning to obtain a patent, the doctrine of prosecution history disclaimer narrows the meaning of the claim consistent with the scope of the claim surrendered. The doctrine of prosecution disclaimer is intended to ensure that claims are not construed one way in order to obtain their allowance and in a different way against accused infringers.

21. I understand that the claims, the specification, and the prosecution history are intrinsic evidence. I understand that courts may also consider extrinsic evidence during claim construction such as expert and inventor testimony, dictionaries, and learned treatises, but that extrinsic evidence is generally given less weight than intrinsic evidence.

B. The Definiteness Requirement

22. I understand that there is a definiteness requirement under 35 U.S.C. § 112, ¶ 2, which requires claims to particularly point out and distinctly claim the invention in the patent. I

understand that a claim is deemed indefinite, and thus invalid, if it fails to inform those skilled in the art about the scope of the invention with reasonable certainty when interpreted in light of the specification and the prosecution history.

V. LEVEL OF ORDINARY SKILL IN THE ART

23. I understand that claim interpretation is from the perspective of a POSITA at the time of the invention.

24. I have been informed that the earliest priority date alleged for the asserted claims of the ’339 Patent, as listed on the cover page of the ’339 Patent, is February 26, 2010.

25. In my opinion, a POSITA at or around the relevant time of the alleged invention would have had at least a Bachelor’s degree in electrical engineering, computer engineering, computer science, or a similar field, as well as at least 2 years of academic or industry experience designing or analyzing electronic circuits, semiconductors, processors, or power management, and related firmware and software, or the equivalent. A POSITA with a higher level of education may have fewer years of academic or industry experience, or vice versa.

26. I was at least a POSITA under this definition as of the alleged priority date.

27. To the extent that Redstone Logics LLC (“Redstone”) or any expert offering testimony on behalf of Redstone puts forward a statement regarding the level of ordinary skill in the art that differs from my opinion above, I reserve the right to respond.

28. Unless otherwise stated, all of my opinions in this Declaration are offered from the perspective of a person of ordinary skill in the art as of the earliest priority date of the ’339 Patent. I had at least the education and experience of a POSITA as of this date by virtue of my approximately (as of that date) two decades training or working in algorithms and architectures for computer processing of data, including the design of hardware for complex processing tasks.

VI. UNDERSTANDING OF THE DISCLOSURE OF THE ASSERTED PATENT

A. U.S. Patent No. 8,549,339

29. The ’339 Patent relates to an arrangement of clock and voltage sources to different groups of processor cores in multi-core processor. ’339 Patent (Ex. A), Abstract; 1:61-2:40. Specifically, the specification describes the use of “power management for a multi-core processor” including a “power profile associated with an individual processor core,” which may include “one or more power-supply voltages of the core processor, clock rates of the core processor, clock multipliers of the core processor, power throttling of the core processor, and/or sleep state cycles of the core processor.” ’339 Patent (Ex. A) at 1:58-2:3.

30. The ’339 Patent also explains that prior art multi-core processors required that “[e]ach processor core in a conventional multi-core processor generally shares the same supply voltage and clock signal to simplify the interfaces between the processor cores.” *Id.* at 1:7-14. The ’339 Patent proposes that each processor core group has an independent power profile powered with a separate supply voltage and that each processor core group obtain a clock output signal from a phase locked loop (PLL) that receives a clock input signal from an “independent clock domain.” *Id.* at 2:27-31, 4:1-17, Fig. 3.

31. This approach is illustrated below in annotated Fig. 3 of the ’339 Patent, which depicts three independent clock signals, “the clock signal 1, the clock signal 2, the clock signal 3” (annotated in green), providing independent inputs to “the respective phase lock loops (PLLs)” 1, 2, and 3. *Id.* at 4:1-17, Fig. 3.

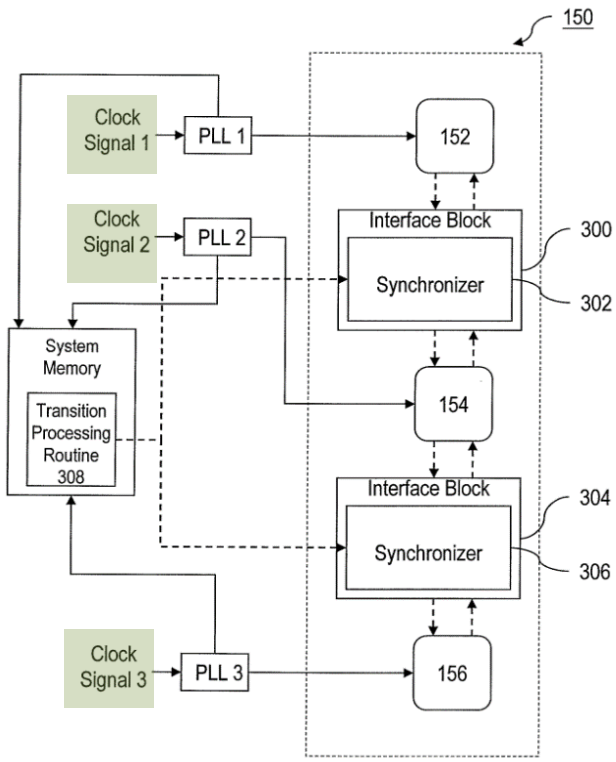


FIG. 3

32. Consistent with Fig. 3, each asserted independent claim (Claims 1 and 21) of the ’339 Patent recites “a first phase lock loop (PLL) having a first clock signal as input” and “a second PLL having a second clock signal as input” wherein “the first clock signal is independent from the second clock signal.” *Id.* at Claims 1 and 21.

VII. DISPUTED TERMS

A. Term 1: “the first clock signal is independent from the second clock signal”

33. I understand that NXP proposes that this term should be construed as having its plain and ordinary meaning, and NXP explains that the plain and ordinary meaning “requires that the first and second clock signals are provided by or processed (i.e., divided or multiplied) from different reference oscillator clocks.” In my opinion, NXP’s proposed construction aligns with

how a POSITA would understand this term in the context of the claims, the specification, and the prosecution history.

34. I understand that Redstone also proposes that the term "the first clock signal is independent from the second clock signal" in the asserted independent claims (Claims 1 and 21) should be construed as having its plain and ordinary meaning, but disputes that this plain meaning requires that the first and second clock signals are provided by or processed (i.e., divided or multiplied) from different reference oscillator clocks. Therefore, it appears that Redstone is interpreting the claim language as broad enough to encompass a first and second clock signal that are provided by or processed (i.e., divided or multiplied) from a single common reference oscillator clock.

1. Prior art processors with a single clock source

35. Computer processors require a clock timing reference to ensure synchronized operation and coordination among its multiple subsystems. These subsystems may include multiple processor cores, memory controllers, and input/output interfaces, all of which rely on the clock to operate in harmony. The clock provides a timing signal that dictates when each core performs computational tasks, accesses memory, or communicates with other components within the processor.

36. The basic design principles for clocks used in processors, including their generation, distribution, and synchronization, were widely known at the time the '339 Patent was filed and documented in technical resources provided by semiconductor manufacturers. This included technical publications, such as application notes and white papers, that often served as references offering detailed insights into clock design methodologies, challenges, and practical implementation tips. For example, ON Semiconductor's application note AND8248/D provides in-depth discussions on the typical path from a reference oscillator clock source to a consumer of

a clock signal. *Stys* (Ex. B) at 1-4. In particular, the disclosure covers crystal oscillators and PLLs, and their role in generating reliable and scalable clock signals for microcontrollers and processors. *Stys* (Ex. B) at 1-4.

37. As shown in annotated Fig. 2 below from *Stys*, the basic design begins with a reference oscillator clock source, typically a crystal oscillator (blue), which generates a stable and accurate reference clock signal (red). *Stys* (Ex. B) at 2, Fig. 2.

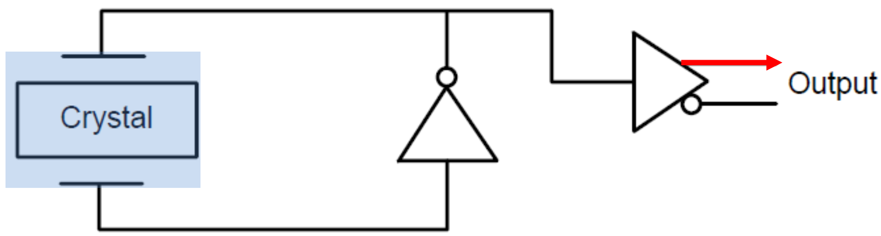


Figure 2. Typical Crystal Oscillator Clock

38. However, there are some limitation with this basic design. The reference clock signal of a standalone crystal oscillator is typically fixed and may not directly meet the wide range of frequency requirements for multi-core processors. This is where a crystal oscillator combined with a PLL provides additional flexibility, as the PLL enables frequency multiplication, division, or fine-tuning to achieve the desired clock frequencies. *Id.* at 1.

39. As shown in annotated Fig. 3 below from *Stys*, the basic PLL design generates precise system clock signals by leveraging an external crystal and a PLL circuit (red). *Id.* at 2-3, Fig. 3. The crystal oscillator (blue) provides the stable reference frequency, which the PLL (red) multiplies or divides to achieve the desired output frequencies. Key components of the PLL, including a gain amplifier, phase frequency detector (PFD), charge pump, low-pass filter (LPF),

and voltage-controlled oscillator (VCO), work together in a feedback loop to align the output signal's phase and frequency with the crystal reference.

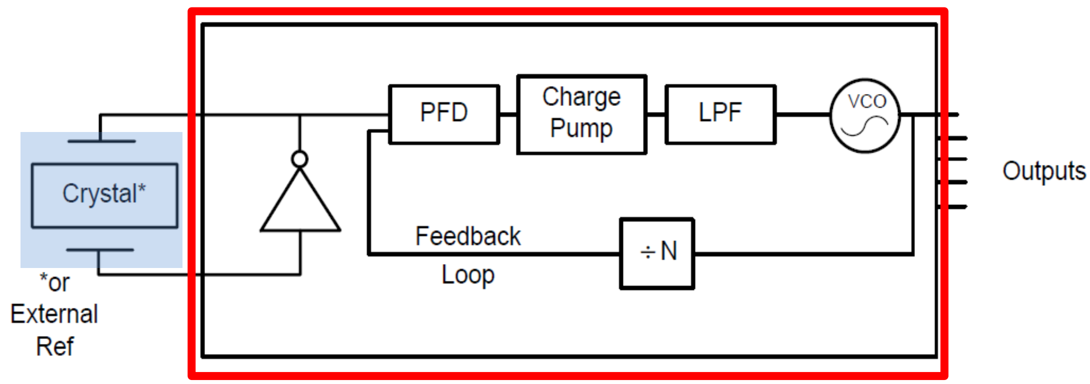


Figure 3. Typical PLL Synthesizer Clock

40. In addition, *Stys* explains that the basic PLL design may include multiple PLLs, dividers, and multipliers, making PLLs versatile for distributing system clock signals. *Id.* at 2-3, Fig. 3. For instance, one divider/multiplier combination might produce a high-frequency clock for a processor core, while another generates a lower-frequency clock for another processor core. *Id.* In such a design, while the PLL can process (e.g., through multiplying/dividing) the reference clock signal to produce multiple different output clock signals, all resulting clock signals are still dependent on the same/single reference oscillator clock. Accordingly, a POSITA would understand that despite the PLL having multiple output clock signals, those output clock signals are not independent because the PLL design still relies on the same/single reference oscillator clock. In other words, when multiple clock signals originate from the same/single reference oscillator clock (as disclosed in the above references), then those clock signals share a dependency and are not independent.

41. Additionally, patents directed to integrated circuits and computer processors frequently detailed known techniques for clock management, including the design and

architectures for clock trees and strategies for optimizing power efficiency. For example, as with the ON Semiconductor's application note AND8248/D, the *Cesky* Patent, assigned to International Business Machines Corporation, describes a typical prior art phase-locked loop design (shown in red box below) that relies on a single reference oscillator clock source (blue). *Cesky* (Ex. C), Fig. 1 (annotated). As shown, the basic phase-locked loop circuit receives a reference clock signal from reference oscillator 102, and includes a phase/frequency detector 104 that generates an error signal that enables adjustments to the VCO's output frequencies to lock in phase and frequency with the reference clock signal. *Id.* at 2:62-3:44. The phase/frequency detector is then coupled to a charge pump 106, a low-pass filter (LPF) 108, and a voltage-controlled oscillator 110. *Id.* at 2:62-3:44, Fig. 1 (annotated).

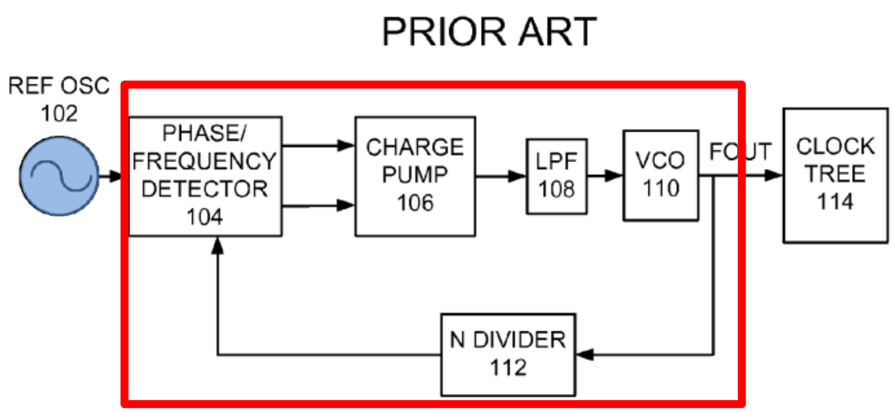


FIG. 1

42. The output clock signals are then distributed (e.g., through a "clock tree" distribution as shown above) within a processor to support various functional blocks (including processor cores) for each subsystem. *Id.* at 2:62-3:44, 4:45-47, Figs. 1, 3; *see also Stys* (Ex. B) at 2-4. *Cesky* is consistent with the teachings of ON Semiconductor's application note AND8248/D as well as other prior art references. For example, *Jacobowitz* is a prior art patent discussed during

the prosecution of the ’339 Patent, which discloses a multi-core processor having a single reference oscillator clock source (112 in Fig. 1) that provides a reference clock signal that is then distributed to the cores. *Jacobowitz* (Ex. D) at [0025], [0037], [0038], [0040], Figs. 1, 5, 6. Similarly, *Kim* is a prior art patent discussed during the prosecution of the ’339 Patent, which discloses a multi-core processor having a single reference oscillator clock source (170 in Fig. 1 and 270 in Fig. 2) that provides a reference clock signal (172 in Fig. 1 and 272 in Fig. 2) that is then processed (i.e., divided or multiplied) to produce different output clock signals for the cores. *Kim* (Ex. E) at [0024]-[0025], Figs. 1-2. I discuss both *Jacobowitz* and *Kim* in the following section.

43. Finally, the ’339 Patent specification explains that “a conventional multi-core processor generally ***shares the same supply voltage and clock signal*** to simplify the interfaces between the processor cores.” ’339 Patent (Ex. A) at 1:7-14 (emphasis added). For these “same clock signal” processors, a POSITA would understand that the clock signals share a dependency from a single reference oscillator clock, as described above, and thus are not independent.

2. During prosecution, the applicant added the phrase “the first clock signal is independent from the second clock signal” to distinguish prior art disclosing multiple clock signals sharing a single reference oscillator clock

44. During prosecution, the examiner rejected the then-pending claims over multiple prior art references including *Jacobowitz* and *Kim*. *See* Ex. F at 4-9 (Office Action (Aug. 29, 2012)). In response, the applicant conducted an examiner interview and explained that *Jacobowitz* “disclosed using ***a single reference clock***,” which was different than FIG. 3 of the ’339 Patent where “clock signals 1 through 3 were ***different/independent clock signals*** input to the PLLs.” *See* Ex. G at 2 (Examiner Interview (Nov. 27, 2012)) (emphasis added). “The examiner ***agreed*** that Jacobowitz discloses using ***a single reference clock***,” but concluded that “the broadest reasonable interpretation of the recited claim language” in the then-pending claims did not exclude

such an arrangement." *Id*. "Applicant's representative stated that he would discuss amends to the claims." *Id.*

45. Two days later, the applicant filed a response amending the independent claims to add the phrase "the first clock signal is independent from the second clock signal" and pointed to that language to distinguish both the *Jacobowitz* and *Kim*. *See* Ex. H at 3, 5-7 (Applicant's Resp. (Nov. 29, 2012)).

46. The applicant explained that "Jacobowitz does not teach or suggest one or more elements of the amended independent claims 1 and 21… Jacobowitz does not teach or suggest at least the elements of…wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal." *Id.* at 9. In particular, the applicant asserted that "FIG. 6 and all other figures of Jacobowitz clearly show that the microprocessor chip (e.g., 600) receives a system reference oscillator clock frequency (VR) and distributes VR to local oscillators 108." *Id*. Based on Jacobowitz's disclosure of use of a ***single*** "reference oscillator clock frequency (VR)," the applicant asserted that "Jacobowitz fails to disclose or teach . . . the first clock signal is ***independent*** from the second clock signal, as required in the amended independent claims 1 and 21." *Id*. at 9-10 (emphasis added); *see also id*. at 11 ("As discussed above, neither Jacobowitz nor Kim discloses having sets of processor cores configured to receive multiple and independent clock signals."). Consistent with this argument, a POSITA would understand the plain and ordinary meaning of "independent" as used the '339 Patent and that the added phrase to the amended claims excludes multiple clock signals (e.g., local oscillators 108) that originate from a single common reference oscillator clock (e.g., reference oscillator clock frequency (VR) originating from "reference oscillator 112").

47. Fig. 1 and 6 from *Jacobowitz* are reproduced below. As shown in annotated Fig. 1 below, *Jacobowitz* discloses a single reference oscillator design that provides a reference clock signal (V_R) (red) from the master reference oscillator (112) (blue). This reference clock signal (V_R) is then distributed throughout various processor embodiments shown in Figs. 1-6. For example, as shown in annotated Fig. 6 below, the 2nd Level Distribution Function (502) distributes reference clock signal (V_R) throughout the processor to two different groups of cores (e.g., group 1 (orange) and group 2 (purple).

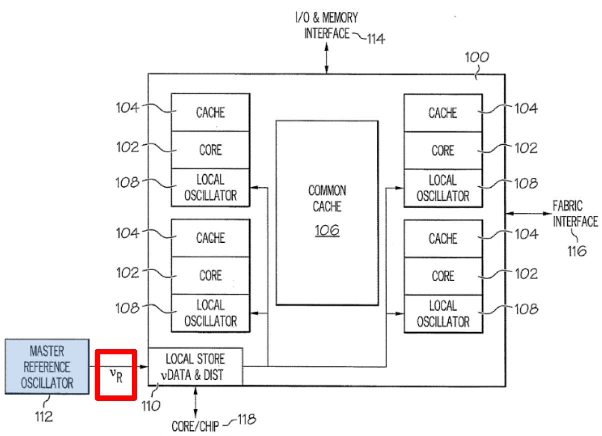


FIG. 1

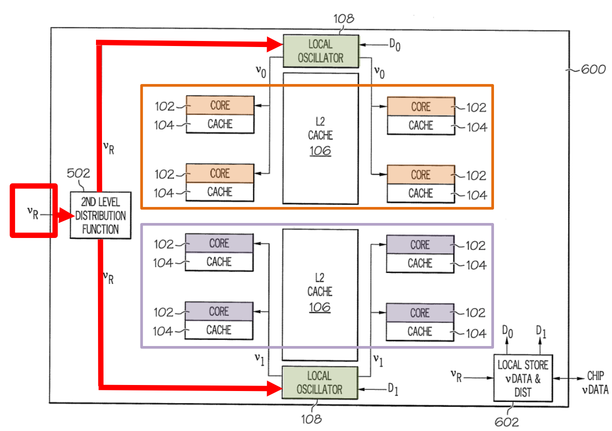


FIG. 6

48. More specifically, as shown in *Jacobowitz* Fig. 6 above, the processor (600) receives the reference clock signal (**V_R**) from the master reference oscillator (112) and distributes **V_R** to local oscillators 108 (green). *See Jacobowitz*, at ¶¶ [0037]-[0038]. Each local oscillator (108) then distributes clock signals to cores (102) (orange/purple) in respective groups of cores. Because the clock signals provided to the processor cores all originate from the same/single reference oscillator clock source (112), a POSITA would understand that the distributed clock signals are not "independent" as used in the '339 Patent. This understanding is consistent with the examiner's and applicant's discussion of "independent" clock signals.

49. With respect to the *Kim* reference, the applicant likewise explained that "Kim also fails to disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal, respectively. In addition, ***the first clock signal is independent from the second clock signal***." *See* Ex. H at 10 (Applicant's Resp. (Nov. 29, 2012)) (emphasis added); *see also id.* at 11 ("As discussed above, neither Jacobowitz nor Kim discloses having sets of processor cores configured to receive multiple and independent clock signals."). "***Instead,*** Kim discloses the apparatus comprising a multi-core processor (i.e., 100 in FIG. 1 or 200 in FIG. 2) having ***a single clock source*** (i.e., 170 in FIG. 1 or 270 in FIG. 2). The clock signal from this single clock source is then ***processed (i.e., divided or multiplied)*** and provided to each of the cores. *See Kim* at ¶¶ [0024]-[0025] and FIGs 1 - 2." *Id.* at 10-11 (emphasis added). Consistent with this argument, a POSITA would understand the plain and ordinary meaning of "independent" as used the '339 Patent and that the added phrase to the amended claims excludes multiple clock signals "processed (i.e., divided or multiplied)" from a single clock source (e.g., clock source 170, which may be "a crystal oscillator").

50. Figures 1 and 2 illustrate two different embodiments from Kim that are reproduced below. Each figure includes a single reference oscillator (blue) that provides an input clock signal (red) to a phased locked loop (PLL) (160 or 260) (green). *See Kim* (Ex. E) at [0024]-[0025] (explaining that clock source 170 or 270 (blue) may be "a crystal oscillator" that provides an "input clock frequency" to a "main PLL 160/260" (green)).

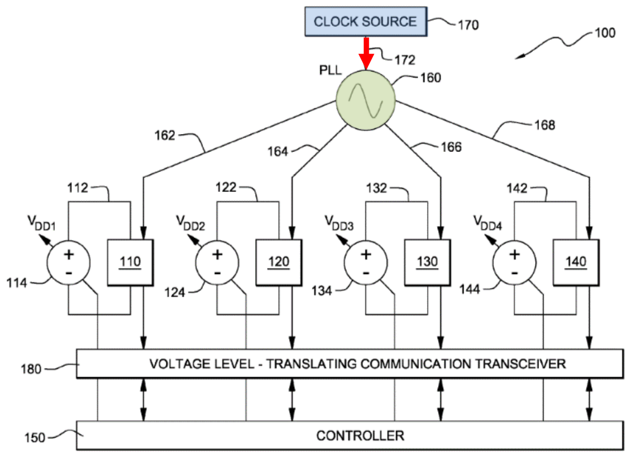


FIG. 1

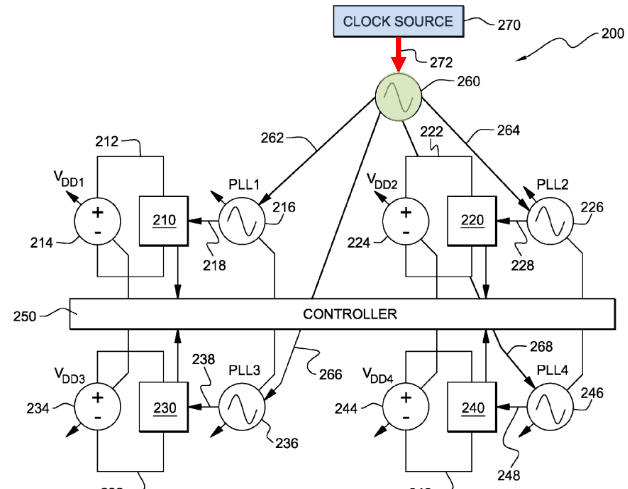


FIG. 2

51. Kim further explains that the reference clock signal (provided by the single reference oscillator clock source) may be further divided by a "main PLL 160 compris[ing]…one or more frequency dividers (preferably, at least one divider for each core in the multi-core processor)…such that, a respective reference input clock frequency (indicated by arrows 162, 164, 166 and 168) is provided to each of the cores in the multi-core processor." *Id.* at [0024]; *see also id.* at [0025] (stating that the main PLL "reference numeral 260, which is configured to receive an input clock frequency from a clock source 270, such as, a crystal oscillator (as shown in FIG. 1)…[and] comprises…one or more frequency dividers"). By dividing or multiplying the reference clock signal received by the main PLL (160/260), multiple, different clock signals may be provided to cores within the processor, where each of these clock signals share a common reference oscillator clock source. *See id.* at Fig. 2, [0025] (stating that each additional PLLs "receives an input clock frequency from the main PLL 260 (indicated by respective arrows 262, 264, 266 and 268), which provides a first multiple of the clock frequency provided by the clock source 270").

52. That is, while *Kim*'s main PLL can divide/multiply the input reference clock signal to produce multiple different clock signals at various frequencies, all clock signals are still

dependent on the same/single reference oscillator clock 170/270. Accordingly, a POSITA would understand that *Kim*'s different clock signals (e.g., 162, 164, 166, 168 / 262, 264, 266, 268) are not independent because each still relies on the same/single reference oscillator clock.

53. In sum, the applicant repeatedly emphasized that regardless of how a reference clock signal reaches the cores (whether provided by or processed (i.e., divided or multiplied) as disclosed in *Jacobowitz* and *Kim*), the added "independent" clock limitation meant that the first clock signal and the second clock signal originated from *different reference oscillator clocks*. *See* Ex. H at 9-11 (Applicant's Resp. (Nov. 29, 2012)). As I explained above, these prosecution statements are consistent with how a POSITA would understand the plain and ordinary meaning of "independent" as used the '339 Patent and that phrase.

54. Consistent with the applicant's discussion, the prior art, and the discussion above, it is my opinion that term "the first clock signal is independent from the second clock signal" should be construed as having its plain and ordinary meaning, "requires that the first and second clock signals are provided by or processed (i.e., divided or multiplied) from different reference oscillator clocks."

B. Term 2: "each processor core from the first/second set of processor cores is configured to dynamically receive a first/second supply voltage [from a power control block] and a first/second output clock signal"

55. I understand that Redstone proposes that the term "each processor core from the first/second set of processor cores is configured to dynamically receive a first/second supply voltage [from a power control block] and a first/second output clock signal" in Claims 1 and 21 should be construed as having its plain and ordinary meaning.

56. I understand that NXP contends this term is indefinite. In my opinion, a POSITA would not be able to determine with reasonable certainty the scope of the term "each processor core from the first/second set of processor cores is configured to dynamically receive a first/second

supply voltage [from a power control block] and a first/second output clock signal" within the context of the '339 Patent.

57. The terms "each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal" and "each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal" appear in Claim 1 of the '339 Patent.

58. For context, Claim 1 of the '339 Patent recites:

> a first set of processor cores of the multi-core processor, wherein **each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal** of a first phase lock loop (PLL) having a first clock signal as input;
>
> a second set of processor cores of the multi-core processor, wherein **each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal** of a second PLL having a second clock signal as input, …

59. The terms "each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage from a power control block and a first output clock signal" and "each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage from a power control block and a second output clock signal" also appear in Claim 21 of the '339 Patent.

60. For context, Claim 21 of the '339 Patent recites:

> a first set of processor cores of the multi-core processor, wherein **each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage from a power control block and a first output clock signal** from a first phase lock loop (PLL) having a first clock signal as input in a clock control block;
>
> a second set of processor cores of the multi-core processor, wherein **each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage from the power control block and a second**

> **output clock signal** from a second PLL having a second clock signal as input in the clock control block, …

61. In my opinion, neither the claims, the specification, nor the ’339 Patent’s prosecution history provide guidance on how a processor core can be—or the meaning of—“configured to dynamically receive” a voltage or clock signal, and that phrase does not have a common understanding in the relevant field.

62. The phrase “configured to dynamically receive” is used only in the claims of the ’339 Patent and not anywhere else in the specification. (As I explain below, the term “dynamic” appears twice in the specification, but in contexts other than dynamically receiving.) These claims require that each processor core is configured to ***dynamically*** receive a supply voltage from a power control block and an output clock signal from a PLL.

63. A POSITA would understand that a typical processor core is capable of receiving signals, including voltages and clock signals. A POSITA would further understand that the ability to receive such signals is a common attribute of processor cores that is required for them to function. This common behavior is reflected in dependent Claims 5 and 14, which recite “wherein the first set of processor cores and the second set of processor cores ***are configured to receive*** one or more control signals from one or more control blocks.” A POSITA would not understand, however, how “configured to ***dynamically*** receive” voltage and clock signals in Claims 1 and 21 is distinguished from receiving voltage and clock signals non-dynamically.

64. The ’339 Patent is silent on how a set of processor cores configured to dynamically receive differs from a set of processor cores that is simply configured to receive. A POSITA trying to avoid Claims 1 and 21 by designing a system that is configured to receive voltage and clock signals, but not configured to dynamically receive the same, would not know what configuration was needed. That is, a POSITA would not understand with reasonable certainty when a processor

core ***is*** configured to dynamically receive these signals and when it ***is not*** within the context of these claims and the patent's specification.

65. In my opinion, in the context of the '339 Patent, "configured to dynamically receive" a signal must mean more than simply being configured to receive a signal that changes over time. In the context of the '339 Patent, however, it is unclear what that something "more" must be, as the specification and claims do not describe or dictate any particular configuration of the processor cores needed for them to "dynamically receive" anything. Specifically, while the term "dynamic" is used twice in the specification, such use is never in reference to the processor cores receiving a signal. '339 Patent (Ex. A), 1:10-14, 3:17-20.

66. First, the specification describes "power consumption management" in a conventional multi-core processor using "dynamic supply voltage and clock speed control" to allow a multi-core processor to "operate at high power and high clock frequency when needed and at low power when the computing requirements are reduced." *Id.* (Ex. A), 1:10-14. This disclosure, which is in the Background of the Disclosure section, simply places the word "dynamic" in front of "supply voltage and clock speed control," and is silent on how the sets of processor cores may themselves be "configured to dynamically receive a first supply voltage and a first output clock signal" or the scope of this phrase.

67. Second, in describing Figure 1, the specification describes "dynamically adjusting the power profile for a stripe in response to changes in computational requirements." *Id.* (Ex. A), 3:17-20. I understand this disclosure as a discussion of power profile adjustments carried out by the control blocks of the multi-core processor (shown in red below in annotated Figure 1 from the '339 Patent). For example, the specification states that the processor cores "may be associated with

an independent power profile" and control blocks select power profiles for the processor cores "based on computational requirements." *Id.* at 2:26-31, 2:41-60.

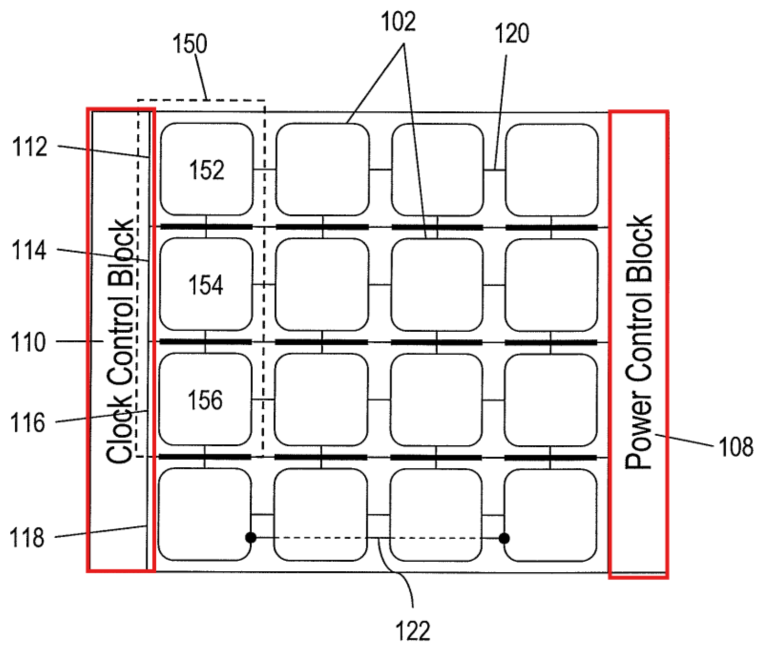


FIG. 1

Id. at Fig. 1 (excerpted, annotated). But again, this disclosure provides no information about how the specific sets of processor cores must be configured in order to dynamically receive signals.

68. Simply put, a POSITA reading the '339 Patent would not understand what differences distinguish a set of processor cores that is configured to dynamically receive a supply voltage or clock signal and one that is not configured to dynamically receive such signals.

69. Thus, it is my opinion that a POSITA cannot determine, with reasonable certainty in view of the specification, the bounds of the claimed invention.

C. Term 3: "located in a periphery of the multi-core processor"

70. I understand that Redstone proposes that the term "located in a periphery of the multi-core processor" should be construed as having its plain and ordinary meaning.

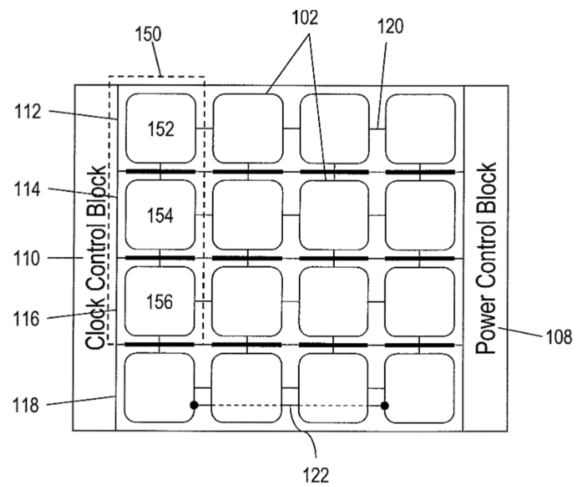
71. I understand that NXP contends this term is indefinite. In my opinion, a POSITA would not be able to determine with reasonable certainty the scope of the term "located in a periphery of the multi-core processor" within the context of the '339 Patent.

72. The term "located in a periphery of the multi-core processor" appears in Claim 5 of the '339 Patent, which depends from Claim 1.

73. For context, Claim 5 of the '339 Patent recites:

> 5. The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks **located in a periphery of the multi-core processor**.

74. In my opinion, neither the claims, the specification, nor the prosecution history provide guidance sufficient to determine whether a location is "in the periphery of the multi-core processor." Further, as described below in greater detail, while a POSITA understands that there are processors with multiple cores, the POSITA would also recognize that the term "multi-core processor" might refer to multiple things. Thus, there is not a common understanding in the relevant field such that a POSITA could determine with reasonable certainty what constitutes the "periphery" of a "multi-core processor."



’339 Patent, Figure 1 (excerpt)

75. Figure 1 of the ’339 Patent is reproduced above. While the patent describes Figure 1 as depicting “an example configuration of a multi-core processor” (*Id.* at 1:26-27), a POSITA understands that the processor cores in a multi-core processor are contained with a die formed on a semiconductor substate, and that the die contains functional blocks in addition to processor cores, and is typically further packaged in plastic and electrical contacts added. Demonstrative Figure A below depicts this arrangement, with ’339 Patent Figure 1’s cores manufactured on a die which itself is encased in protective packaging.

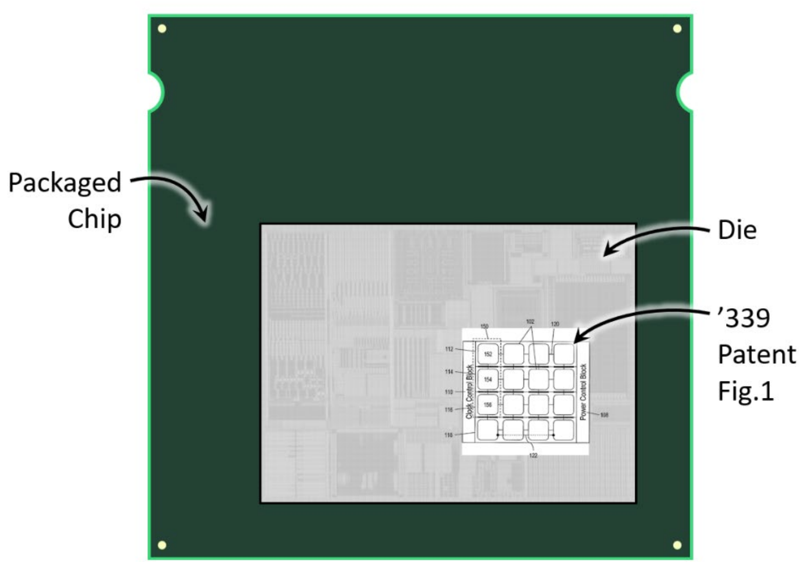


Figure A

76. As noted above, A POSITA understands there is no single understanding of "multi-core processor." In some instances, a POSITA might refer to the multiple individual processor cores (such as processor cores 152, 154, and 156 in Figure 1) as a multi-core processor. In other instances, a POSITA may consider the complete die, containing the processor cores and additional circuitry—for example, PLLs, power amplifiers, memory, and RF components—as a "multi-core processor." Still, a POSITA may also refer to the packaged die as a "multi-core processor." Demonstrative Figure B is an annotated version of Figure A with the border of each such interpretation of multi-core processor highlighted in a different color:

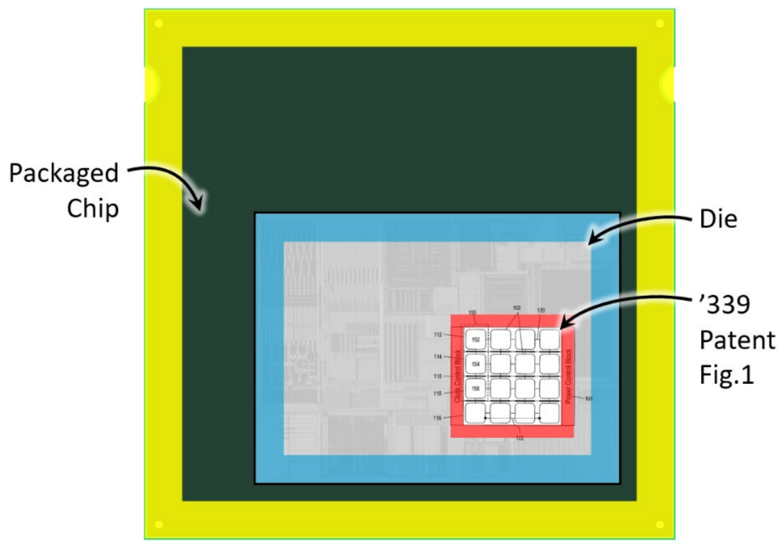


Figure B

77. The red rectangle in Figure B denotes the boundary of just the processor cores of Figure 1; the blue rectangle denotes the boundary of the die; and the yellow rectangle denotes the boundary of the packaged die. A POSITA would not be reasonably certain, based on the claim language, which if any of the three depicted boundaries should be used to identify the periphery required in dependent Claim 5. For example, the POSITA would not know whether some or all of the components located outside the red boundary but within the blue boundary are within the "periphery." The POSITA would also be unsure whether the "periphery" might refer to everything

outside the red boundary but within the yellow boundary, or whether "periphery" might include, or be limited to, components outside the yellow boundary.

78. Thus, it is my opinion that a POSITA cannot determine, with reasonable certainty in view of the claims, the meaning of the phrase "located in a periphery of the multi-core processor."

79. The '339 Patent's specification does not resolve the ambiguity. As described in the patent, "FIG. 1 illustrates an example configuration of a multi-core processor 100…. The multi-core processor 100 may include multiple processor cores 102 arranged in rows and columns in a 2-dimensional array in an integrated circuit." '339 Patent (Ex. A), 2:4-9. "Each row of processors may also be referred to as a 'stripe.' For example, the multi-core processor 100 may be divided into stripes 112, 114, 116, and 118. Each stripe may be associated with an independent power profile." *Id.* at 2:24-27. A POSITA would understand that each stripe of Figure 1 is an example of the set of processor cores from independent Claims 1 and 21.

80. The specification further describes control blocks located "at two different sides of the multi-core processor 100 as shown in FIG. 1," "at the same side of the multi-core processor 100," or "in a common area located near the center of the multi-core processor 100." *Id.* at 2:31-40. However, it is unclear whether or not any of these described locations are considered "in a periphery" of the claimed multi-core processor. This lack of clarity is further underscored by the labeling (in the upper left of the figure) of the *entirety* of Figure 1 as a multi-core processor. *Id.* at 2:4-5. This leaves it unclear whether "periphery of the multi-core processor" might be limited to regions *inside* the multi-core processor within some unspecified distance of the boundary of the multi-core processor, however that boundary might be defined, or whether "periphery of the multi-

core processor" also includes components outside the multi-core processor but within some unspecified distance of its boundary.

81. The description in the specification of the components depicted in Figure 1 as a "multi-core processor" (*id.*) does not resolve the ambiguity. Although the '339 Patent depicts multiple processor cores as physically arranged adjacent each other in rows and columns, neither of independent Claims 1 and 21 nor dependent Claim 5 require the first and second sets to be arranged in adjacent rows, columns, or a grid. A POSITA would understand that that the processor cores of a multi-core processor need not be located immediately adjacent to one another in the manner depicted in the patent's Figure 1. Rather, the first set of processor cores and the second set of processor cores of the claims could be spaced apart on the semiconductor die, as depicted in Demonstrative Figure C.

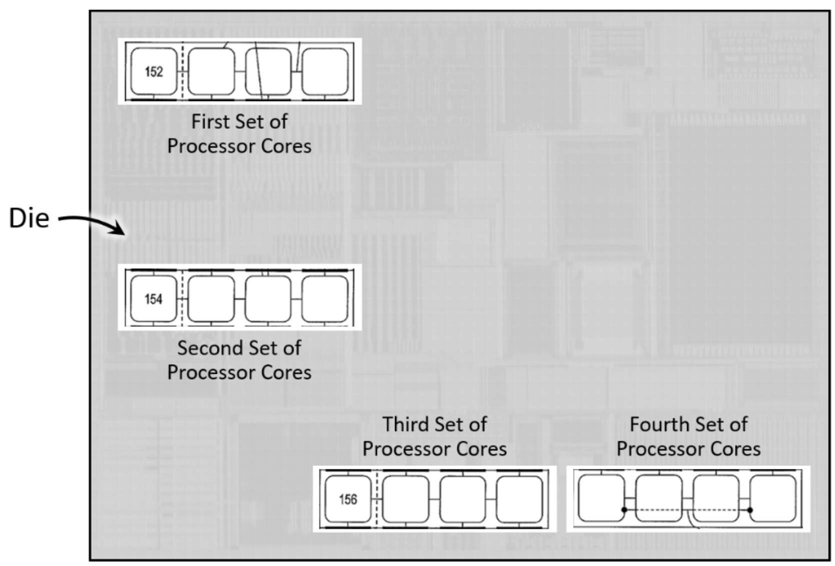


Figure C

82. Figure C modifies Figure 1 from the patent such that each of the stripes is spaced apart on the die, and the voltage and control blocks are omitted. If one views the collection of processor cores alone as the "multi-core processor" of the claims, with the stripes of Figure 1

arranged in the manner depicted in Figure C, a POSITA would not understand with reasonable certainty what constitutes the periphery of such a multi-core processor.

83. Thus, it is my opinion that a POSITA cannot determine, with reasonable certainty in view of the claims and the specification, the scope of the phrase "located in a periphery of the multi-core processor."

D. Term 4: "located in a common region that is substantially central to the first set of processor cores and the second set of processor cores"

84. I understand that Redstone proposes that the term "located in a common region that is substantially central to the first set of processor cores and the second set of processor cores" should be construed as having its plain and ordinary meaning.

85. I understand that NXP contends this term is indefinite within the context of the '339 Patent. In my opinion, a POSITA would not be able to determine with reasonable certainty the scope of the term "located in a common region that is substantially central to the first set of processor cores and the second set of processor cores" within the context of the '339 Patent.

86. The term "located in a common region that is substantially central to the first set of processor cores and the second set of processor cores" appears in Claim 14 of the '339 Patent, which depends from Claim 1.

87. For context, Claim 14 of the '339 Patent recites:

> 14. The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks **located in a common region that is substantially central to the first set of processor cores and the second set of processor cores**.

88. In my opinion, neither the claims, the specification, nor the prosecution history provide guidance on how to determine whether a region is "common" or whether a region is "substantially central" to the processor cores. Further, neither "located in a common region" nor

"substantially central" have a common understanding in the relevant field such that a POSITA could determine with reasonably certainty what constitutes components "located in a common region" or whether such components are "substantially central" to the first and second sets of processor cores.

89. In my opinion, the claim language provides no clarity as to what constitutes a common region. Claim 14 recites, in part, "the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region." Thus, the claim requires that the "common region" is a "region" of processor cores that is "common" to both the first set of processor cores and the second set of processor cores and that further contains one more control blocks.

90. But this still leaves significant ambiguity. Among other challenges, identifying a "common region" first requires identifying what the patentee means by "region"—a term that, as used herein, compounds rather than resolves ambiguity. The lack of clarity is further underscored by the language of Claim 8, which like Claim 14 depends directly (without any intervening dependent claims) from Claim 1. Claim 8 describes the processor cores as located in a "region." Specifically, Claim 8 states "the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor."

91. But, the disclosure of regions containing the first and second sets of processor cores in Claim 8 would not provide a POSITA with reasonable certainty regarding what delineates a region or what it means for such a "region" to be "common" between the first and second sets of processor cores. Absent further guidance, one interpretation of "common" in this context would be regions that overlap each other. But "overlapping" regions are explicitly claimed in Claim 9,

which depends from Claim 8 and states, in part, "wherein the first region and the second region are overlapping regions." A POSITA would note that the patentee, by using "overlapping" in Claim 8 and "common" in Claim 14, distinguished between "overlap" and "common," though the nature of such a distinction is never made clear.

92. In my opinion, the specification does not resolve the lack of clarity regarding "common region." The phrase "common region" is never used in the patent's specification. While the specification does use the phrase "common area," that use is within the context of control blocks being in the same area, as opposed to a region that is "common" to the first and second sets of processor cores, as the claim requires. Specifically, the specification states "[i]n yet some other implementations, the power control block 108 and the clock control block 110 may be arranged in a common area located near the center of the multi-core processor 100." *Id.* at 2:37-40. A POSITA would not understand the "common region" language of Claim 14 to refer to the "common area" of the specification because the cited portion of the specification refers to <u>two</u> control blocks—the power and clock control blocks—as being located in the same area. Such a scenario is not co-extensive with Claim 14, which requires that "<u>one</u> or more control blocks [be] located in a common region that is substantially central to" the first and second sets of processor cores. The patent thus leaves unclear how a region with only one control block could be deemed to have another control block in "common." As such, neither the specification nor the claims provides reasonable certainty as to the scope of a "common region."

93. In my opinion, another source of ambiguity is the Claim 14 phrase "substantially central."

94. Neither the claims nor the specification inform a POSITA as to the scope of the phrase "substantially central," nor what it means for a "common region" to be "substantially

central" to the first and second sets of processor cores. Indeed, the phrase "substantially central" is never used in the specification.

95. Claim 14 requires that the region containing "one or more control blocks" is substantially central to the multiple sets of processor cores. An example of control blocks is shown in Demonstrative Figure D. In this image, the clock control block and the power control block are relatively equidistant from each of the sets of processor cores. Furthermore, the clock control block and the power control block are not immediately adjacent to any set of processor cores. Given this placement of processor cores, the POSITA would not know whether the clock control block and the power control block are "substantially central" (on the basis of being placed in the middle of the figure), or not "substantially central" (on the basis of the separation between the control blocks and processor cores to the first and second sets of processor cores).

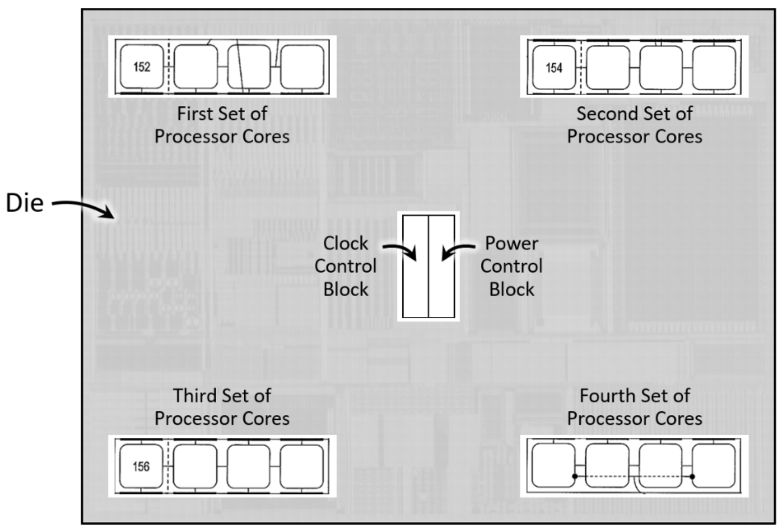


Figure D

96. As substantially central is a term of degree, a POSITA understands that establishing the claim scope requires identifying a position of the control blocks that either would, or would not, be deemed substantially central to the sets of processor cores. To illustrate, Figure D is

simplified in Demonstrative Figure E to include only two stripes from Figure 1, *i.e.*, first and second sets of cores, consistent with the asserted claims.

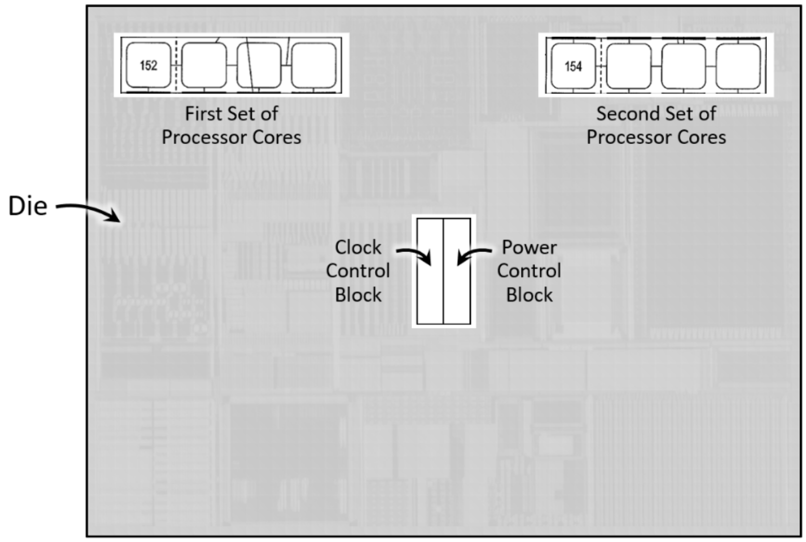


Figure E

97. The clock control block and the power control block in Figure E are located at the horizontal midpoint between the first and second sets of processor cores, but the control blocks lie in a different vertical position than the sets of processor cores. A POSITA would not understand (a) whether the control blocks in Figure E are substantially central to the sets of processor cores because they are at the horizontal midpoint between the sets of processor cores, or (b) whether the control blocks in Figure E are not substantially central because they are below and in a different vertical plane from the sets of processor cores.

98. Thus, it is my opinion that a POSITA cannot determine, with reasonable certainty in view of the specification, the claims, and the prosecution history, the bounds of the term "located in a common region that is substantially central to the first set of processor cores and the second set of processor cores."

I declare under penalty of perjury under the laws of the United States that the foregoing is true and correct to the best of my knowledge.

Executed on the 3rd day of Dec. 2024 in Santa Monica, CA.

By: John Villasenor

Dr. John Villasenor